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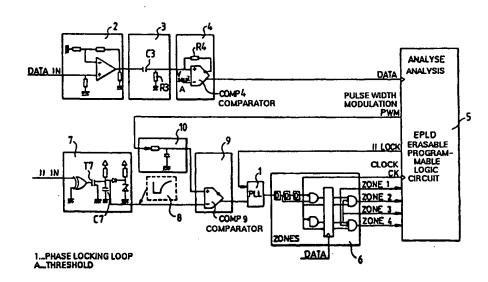
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(54) Title: CLOCK RECOVERY METHOD IN DIGITAL SIGNAL SAMPLING

(54) Titre: PROCEDE DE RECUPERATION D'HORLOGE LORS DE L'ECHANTILLONNAGE DE SIGNAUX DE TYPE NU-MERIQUE

(57) Abstract

The invention concerns a clock recovery method in digital signal sampling, the clock being generated from a phase-locking loop or PLL (1) which multiplies a given frequency by a whole number. Said method comprises a step which consists in comparing the relative position of the signals with respect to the clock so as to determine whether a selected type of the clock transitions is in phase with the same type of signal transitions by: producing (6) over a clock period several zones, one zone corresponding to the selected type of transitions; analysing (5) the signal transitions relatively to the clock uplink or



downlink transitions; cumulating in the corresponding zone the analysis results; determining (10, 9) on the basis of the accumulation whether the sampling clock frequency and/or phase needs to be modified or not. The invention is applicable to signals derived from graphics cards.